REMARKS

Claims 1-14 and 60-88 are pending. Claims 60, 65, and 72-74 are rejected under 35 U.S.C. § 112, second paragraph. Claims 1-12, 14, 60-84 are rejected under 35 U.S.C. § 103(a). Claims 1, 60, and 72-74 have been amended. Claims 28-35 and 89-107 are canceled without prejudice.

Ronald Neerings (Reg. No. 34,227) has made a provisional election of Group I claims 1-14 and 60-88 in response to Examiner's restriction requirement. Applicants hereby affirm the election of Group I claims. Group II claims 28-35 and 89-107 are cancelled without prejudice.

Examiner has objected to the Abstract as being too long. Applicants have amended the Abstract to reduce the length and present a narrative description of the present invention.

Examiner has stated that claims 60 and 65 use the term "output" to mean "input" and are, therefore, contradictory. Applicants respectfully disagree. Input terminals receive input signals and output terminals receive output signals within their ordinary meaning. This has nothing to do with being a lexicographer or redefining terms. Referring to Figures 3 and 4, for example, claim 60 recites "A circuit *22'*, comprising: an input terminal [at D^1] coupled to receive a first [S_1-S_4] and a second [S_5-S_8] group of signals, each group having a respective sequence; a first output terminal [at D_1^1] coupled to receive the first group of signals during a first time [t_1-t_5]; and a second output terminal [at D_2^1] coupled to receive a third group of signals [$(-S_8)^*$-$(-S_5)^*$] having a sequence during the first time, the third group of signals comprising a transform [negative conjugate] of the second group of signals." Claim 65 recites "A circuit as in claim 60, wherein the first output terminal is coupled to receive the second group of signals [S_5-S_8] during a second time [t_5-t_9], and wherein the second output terminal is coupled to receive a fourth group of signals [$(-S_4)^*$-$(-S_1)^*$] having a sequence during the second time, the fourth group of signals comprising a transform [conjugate] of the first group of signals." (identification added). Thus, applicants believe terms of claims 60 and 65 and related claims are clear and within their ordinary meaning. Applicants submit that claims 60-77, therefore, are patentable under 35 U.S.C. § 112, second paragraph.

Examiner has identified claims 72-74 as lacking antecedent basis for "the channel encoder circuit." Applicants have amended claims 72-74 to depend from claim 71. Thus, claims 72-74 are patentable under 35 U.S.C. § 112, second paragraph.

Independent claims 1, 60, and 78 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ramesh (U.S. Pat. No. 6,256,290) in view of Chen et al. (U.S. Pat. No. 6,304,581). Examiner states that Ramesh fails to teach the reordering of the second symbol groups, but Chen et al. teach a means for reordering the symbols. (Figure 1, block 127). Claim 1, as amended, recites in part "for each of the plurality of different user channels, circuitry for forming a second symbol group sequence by *time reversing symbols* in at least some of the plurality of groups of symbols to form the second symbol group sequence different from the first symbol group sequence." (emphasis added). By way of contrast, Chen et al. teach block 127 performs a circular shift operation by a predetermined number. (col. 2, line 67-col. 3, line 5). Chen et al. DO NOT disclose "time reversing symbols in at least some of the plurality of groups" as required by claim 1. A combination of Ramesh and Chen et al., therefore, fails to disclose all the elements of claim 1. Thus, claim 1 and depending claims 2-14 are patentable under 35 U.S.C. § 103(a) over Ramesh in view of Chen et al.

Moreover, one of ordinary skill in the art would not think to combine Ramesh with Chen et al. to produce the present invention. Chen et al. disclose a method of interleaving data symbols of a block of data symbols. (Abstract). A Block Interleaver is already disclosed by Ramesh at Figure 5, block 505. One of ordinary skill in the art would not think to add a second redundant Block Interleaver of Chen et al. to the Block Interleaver of Ramesh. Moreover, neither Chen et al. nor Ramesh teach or suggest such a combination or a problem that might be solved by such a combination. Thus, claim 1 and depending claims 2-14 are patentable under 35 U.S.C. § 103(a) over Ramesh in view of Chen et al.

Claim 60, as amended, recites "an input terminal coupled to receive a first and a second group of signals, each group having a respective sequence; a first output terminal coupled to receive the first group of signals during a first time; and a second output terminal coupled to receive a third

group of signals having a sequence during the first time, *the third group of signals comprising a transform of the second group of signals, wherein the third group of signals is different from the second group of signals*." By way of example, this feature of the present invention is shown at the embodiment of Figure 4, wherein the first group of signals is S_1-S_4, the second group of signals is S_5-S_8, and the third group of signals is $[(-S_8)^*-(-S_5)^*]$. By way of contrast, Chen et al. fail to disclose a "third group of signals comprising a transform of the second group of signals" as required by claim 60. Moreover, Chen et al. fail to disclose that "the third group of signals is different from the second group of signals." The OTD Interleaver 105 (Figure 1) of Chen et al. only reorders the input symbol sequence. The output symbols, however, remain the same as the input symbols. No signal transform is disclosed by a combination of Ramesh and Chen et al. Thus, claim 60 and depending claims 61-77 are patentable under 35 U.S.C. § 103(a) over Ramesh in view of Chen et al.

Furthermore, one of ordinary skill in the art would not think to combine Ramesh with Chen et al. to produce the present invention. Chen et al. disclose a method of interleaving data symbols of a block of data symbols. (Abstract). A Block Interleaver is already disclosed by Ramesh at Figure 5, block 505. One of ordinary skill in the art would not think to add a second redundant Block Interleaver of Chen et al. to the Block Interleaver of Ramesh. Moreover, neither Chen et al. nor Ramesh teach or suggest such a combination or a problem that might be solved by such a combination. Thus, claim 60 and depending claims 61-77 are patentable under 35 U.S.C. § 103(a) over Ramesh in view of Chen et al.

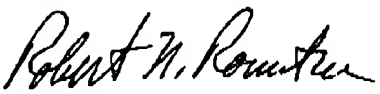
Claim 78 recites "applying a respective plurality of signals to each of a plurality of encoder circuits; producing *a first group* of the respective plurality of signals *at a first output terminal of said each of a plurality of encoder circuits*; producing *a transformed second group* of the respective plurality of signals *at a second output terminal of said each of a plurality of encoder circuits*; and modulating the first group and the transformed second group each of the respective plurality of signals by a respective code corresponding to said each of a plurality of encoder circuits." Examiner admits that Ramesh discloses a plurality of encoder circuits and nothing else. But Ramesh DOES NOT disclose first and second output terminals of Encoder 501. Furthermore, Chen et al. do not disclose the plurality of encoder circuits or Examiner would not have relied on Ramesh. Therefore,

no combination of Ramesh and Chen et al. discloses first and second output terminals of each encoder circuit. Thus, claim 78 and depending claims 79-88 are patentable under 35 U.S.C. § 103(a) over Ramesh in view of Chen et al.

As previously explained, one of ordinary skill in the art would not think to combine Ramesh with Chen et al. to produce the present invention. Chen et al. disclose a method of interleaving data symbols of a block of data symbols. (Abstract). A Block Interleaver is already disclosed by Ramesh at Figure 5, block 505. One of ordinary skill in the art would not think to add a second redundant Block Interleaver of Chen et al. to the Block Interleaver of Ramesh. Moreover, neither Chen et al. nor Ramesh teach or suggest such a combination or a problem that might be solved by such a combination. Thus, claim 78 and depending claims 79-88 are patentable under 35 U.S.C. § 103(a) over Ramesh in view of Chen et al.

In view of the foregoing, applicants respectfully request reconsideration of claims and allowance of claims 1-14 and 60-88. If the Examiner finds any issue that is unresolved, please call applicants' attorney by dialing the telephone number printed below.

Respectfully submitted,



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